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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/810,032	03/26/2004	Steven K. Knapp	X-1421 US	8424

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EXAMINER	
PEUGH, BRIAN R	

ART UNIT	PAPER NUMBER
2187	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	02/07/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/810,032	KNAPP, STEVEN K.	
	Examiner	Art Unit	
	Brian R. Peugh	2187	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 January 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10 and 12-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *9,10 and 12-18* is/are allowed.

6)☒ Claim(s) *1-8* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

This Office Action is in response to applicant's communication filed January 16, 2007, in response to PTO Office Action dated November 15, 2006. The applicant's remarks and amendment to the specification and/or claims were considered with the results that follow.

Claims 1-10 and 12-18 have been presented for examination in this application. Applicant's request for reconsideration of the finality of the rejection of the last Office action is persuasive and, therefore, the finality of that action is withdrawn.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-8 are rejected under 35 U.S.C. 102(e) as being anticipated by Xia et al. (US# 2006/0038586).

Regarding claim 1, Xia et al. teaches a system comprising: a serial flash memory (106); and a programmable logic device (103) having an interface (124) coupled to the

serial flash memory, wherein the interface is configured to identify the serial flash memory [0025; 0029; 0039-0041;].

Regarding claim 2, Xia et al. teaches wherein the serial flash memory operates in accordance with the serial peripheral interface (SPI) protocol [0029].

Regarding claim 3, Xia et al. teaches wherein the serial flash memory is coupled to the interface by a standard SPI four-wire interface [Fig. 3; four of the wires comply with the 'standard'; 0026 & 0027].

Regarding claims 4-7, Xia et al. teaches wherein the programmable logic device further comprises an address register configured to provide a start address to the serial flash memory, wherein the start address identifies an initial address to be accessed in the serial flash memory; means for initially setting the start address to a predetermined address; means for modifying the start address from the predetermined address to another address; and means for updating a configuration of the programmable logic device stored in the serial flash memory during normal operation of the programmable logic device [although not explicitly reciting registers, PLD 103 instructs flash 106 to begin sending configuration data for the PLD, which inherently requires sending an address to the memory from which to start the data transferal process;

Regarding claim 8, Xia et al. teaches, wherein the programmable logic device is a field programmable gate array (FPGA) [0082].

Claims 1-8 are rejected under 35 U.S.C. 102(e) as being anticipated by Tang (US# 7,095,247).

Regarding claim 1, Tang et al. teaches a system comprising: a serial flash memory (304); and a programmable logic device (302) having an interface (306) coupled to the serial flash memory, wherein the interface is configured to identify the serial flash memory [col. 1, lines 34-56].

Regarding claim 2, Tang et al. teaches wherein the serial flash memory operates in accordance with the serial peripheral interface (SPI) protocol [col. 1, lines 50-51].

Regarding claim 3, Tang et al. teaches wherein the serial flash memory is coupled to the interface by a standard SPI four-wire interface [Fig. 3].

Regarding claims 4-7, Tang et al. teaches wherein the programmable logic device further comprises an address register configured to provide a start address to the serial flash memory, wherein the start address identifies an initial address to be accessed in the serial flash memory; means for initially setting the start address to a predetermined address; means for modifying the start address from the predetermined address to another address; and means for updating a configuration of the

programmable logic device stored in the serial flash memory during normal operation of the programmable logic device [although not explicitly reciting registers, FPGA 302 sends requests to FLASH 304 to begin sending configuration data for the FPGA, which inherently requires sending an address to the memory from which to start the data transferal process;

Regarding claim 8, Tang et al. teaches, wherein the programmable logic device is a field programmable gate array (FPGA) [302].

Allowable Subject Matter

Claims 9, 10, and 12-18 are allowed over the prior art of record.

Response to Arguments

Applicant's arguments with respect to claims 1-8 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brian R. Peugh whose telephone number is (571) 272-4199. The examiner can normally be reached on Monday-Thursday from 7:00am to 4:30pm. The examiner can also be reached on alternate Friday's from 7:00am to 4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald Sparks, can be reached on (571) 272-4201. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 571-272-2100.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Brian R. Peugh
Primary Examiner
Art Unit 2187
February 3, 2007